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DESIGN AND IMPLEMENTATION OF MULTI FPGA NETWORK WITHOUT USING BUFFER

R.Vignesh[1], C.Subashini[2]

[1]M.E,S.A.Engineering College,Anna University of Technology, Chennai
[2]S.A.Engineering College, Anna University of Technology, Chennai

E-mail of Corresponding Author: vickyece2@gmail.com

ABSTRACT

As we know mobile and wireless technologies are contributing in development of states, countries and world in many ways .This paper proposes the implementation of mobile in health services in the remote areas of HP. This paper presents the penetration of mobile in the developing countries and their use in the health sector. This paper gives a model of health using mobile cellular communications in the health services. This paper proposes that how the portable biomedical equipment's and telecommunication systems can be combined to provide health services in remote areas with improved patient safety, reduced cost and challenges in doing this.

INTRODUCTION

ROUTING

The system is based on a novel routing concept. The main advantage of this concept is that any possible signal connectivity can be routed on the proposed structure. None of the previously mentioned unused or additional pin penalty can occur. Figure no 1.1 shows the switching network of two FPGAs and one pin each. One FPGA pin of each FPGA is picked and the resulting group is connected via switches to build a switching network.

The switching network generates two intermediate nets on each of the adjacent FPGA layers. On one single switch board multiple of this switching networks can be realized. One pins are occupied in a routing network of one FPGA pin, the pair wise connectivity of intermediate nets allows the connection of this pin to the neighboring network. If this is not possible, the previously routed graph could be modified to use horizontal connections and the connectivity is done on the same network.

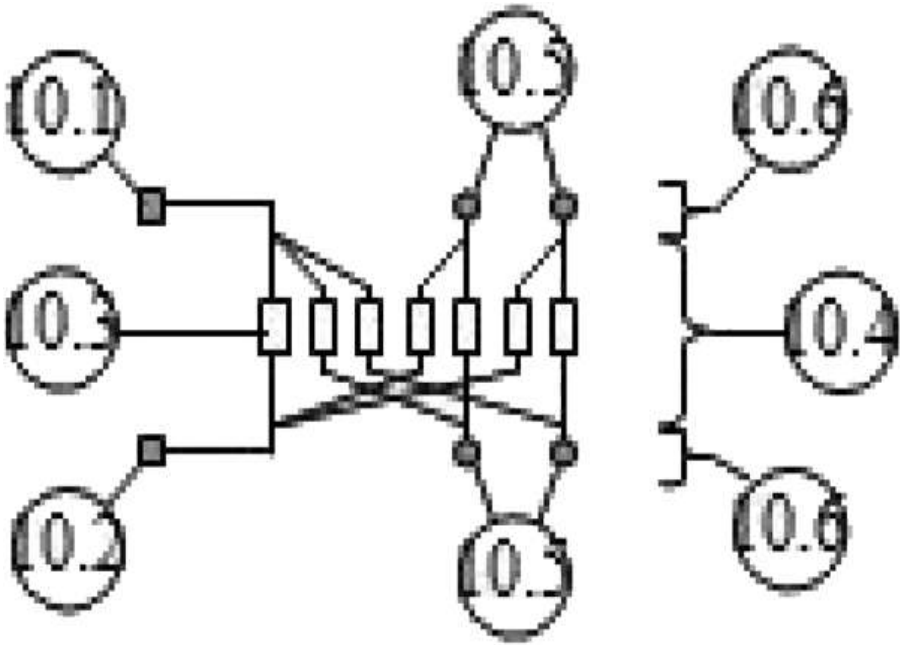


Figure no 1 Switching Network of Two FPGAs (one pin each)

RECONFIGURABLE ARCHITECTURE

Reconfigurable computing is a computer architecture combining some of the flexibility of software with the high performance of hardware by processing with very flexible high speed computing fabrics like field-programmable gate arrays (FPGAs). The principal difference when compared to using ordinary microprocessors is the ability to make substantial changes to the data path itself in addition to the control flow. On the other hand, the main difference with custom hardware, i.e. application-specific integrated circuits (ASICs) is the possibility to adapt the hardware during runtime by "loading" a new circuit on the reconfigurable fabric. The reconfigurable computers can be categorized in two classes of architectures: hybrid computer and fully FPGA based computers. Both architectures are designed to transport the benefits of reconfigurable logic to large scale computing. They can be used in traditional CPU cluster computers and network infra structures.

Delay Variation

In alternative concepts between FPGAs can vary by a great range. This is mainly due to the resulting different length of paths, when a planar orientated FPGA placement is done. Routing 1200 signals with equal length between four FPGAs seems to be impossible. If switching technology is used, the routing effort becomes even more critical due to fast rising number of routing/switching devices on the board. Especially if pass transistor based switching technology is used, different wire length and their different capacities change the slope.

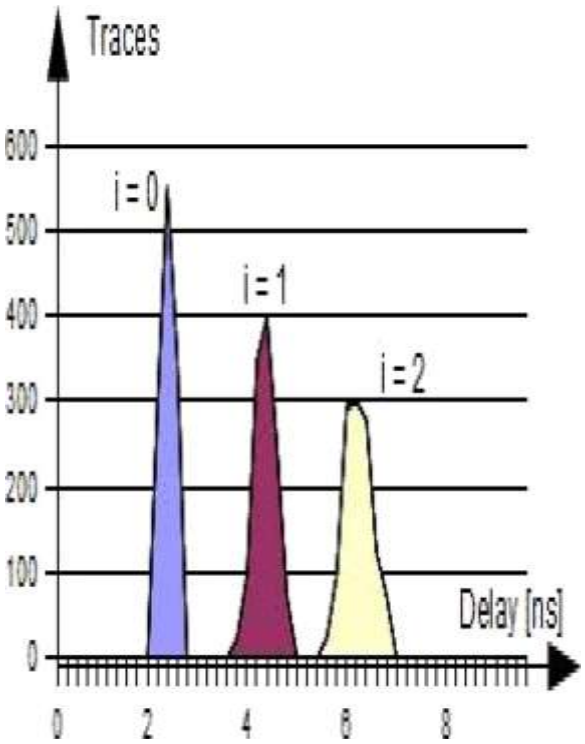


Fig no 2 Delay Variation Concentric Structure

The clock edge arrives at the same time as the data signals at the FPGA pins. The constant insertion delay (signal traveling from the I/O-pin of the clock tree to the individual clock input of the registers) of the FPGA clock trees and constant setup and hold times of registers (placed at the I/O-blocks) guarantee that the results can be reproduced. The receiving data block is split

In to rising edge and falling edge receiving registers so that both edges of the parallel routed clock can be used .A self-timed wave-pipelined structure simplifies the efforts to guarantee a working solution. The clock signal is only routed to the sending blocks and replaces the low-skew global clocks. A clock is generated by the sending FPGA and is sent out in parallel to the data signals.

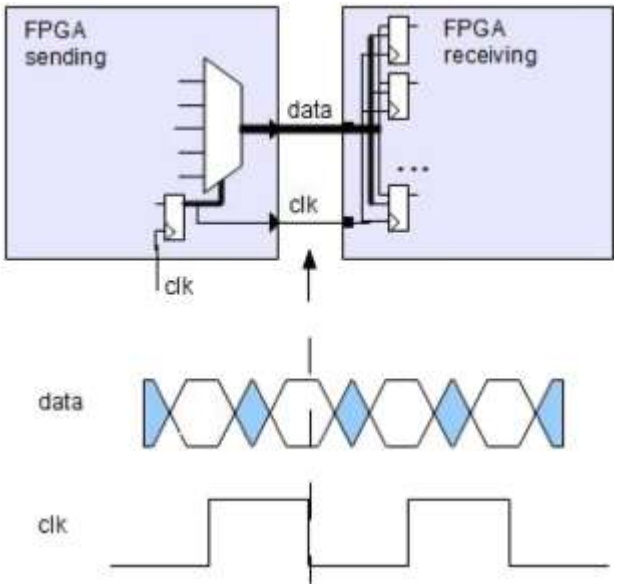
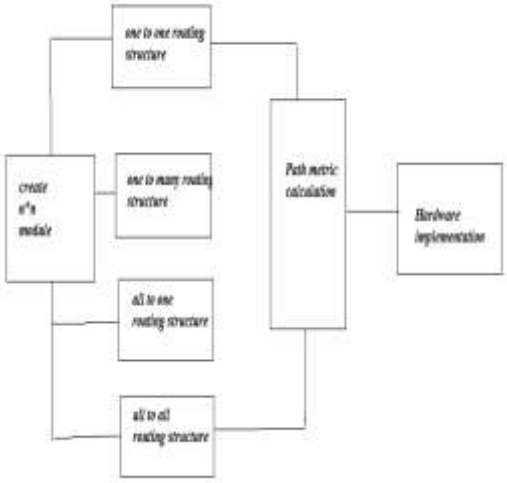


Fig no 3 Delay Structure

In almost all cases, FPGAs have sending and receiving modules at the same time. This is why system level clocks are lo skew signals. An additional critical signal is the reset signal, which resets the counter modules of both sending and receiving blocks of source and target FPGAs.

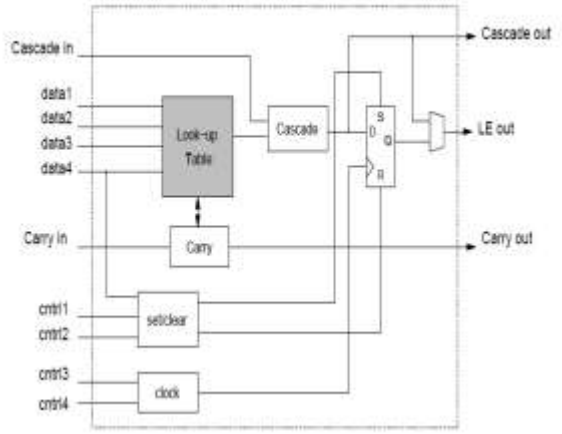
If this reset signal does not become inactive at the same clock cycle on both sides, the counting is not in sync and a system malfunction is guaranteed. To avoid false mapping of sending and receiving data due to incorrect pointer counting the corresponding select information of the data is also transferred.

IV Path Identifier



Create n*n modules that is among no of nodes routing take place among them dynamically nodes are selected, Switching technology is implemented to reduce the inter connections and to reduce delay between nodes. Then Routing path metric is calculated Routing is done in four ways One to One Routing, One to Many Routing, All to one routing and All to all routing solve compute intensive problems and also in the verification and prototyping of large circuits. This paper addresses the problem of routing multi-terminal nets in a multi-FPGA system that uses partial crossbars as interconnect structures. The multi-terminal routing problem is first modeled as a partitioned bin packing problem and formulated as an integer linear programming problem where the number of variables is exponential, Compute an upper bound on the routing solution.

Fig no 5 Look up Table



The FPGA is an array or island-style FPGA. It consists of an array of logic blocks and routing channels. Two I/O pads fit into the height of one row or the width of one column, as shown below. All the routing channels have the same width (number of wires). Data is given as input to LUT which is cascaded to SR FLIPFLOP CTRL bits are given to set and clear flip flop data Carry generator is provided to take carry in and out Multiplexer is provided to select the inputs. Each circuit must be mapped into the smallest square FPGA that can accommodate it. The FPGA logic block consists of a 4-input look-up table (LUT), and a flip flop, as shown below. There is only one output, which can be either the registered or the unregistered LUT output. The logic block has four inputs for the LUT and a clock input. Since the clock is normally routed via a special-purpose dedicated routing network in commercial FPGAs, do NOT route it or include it in your track count results. That is, you can completely ignore the clock net, since it is assumed to be routed on a special global network.

COMPARISON RESULTS

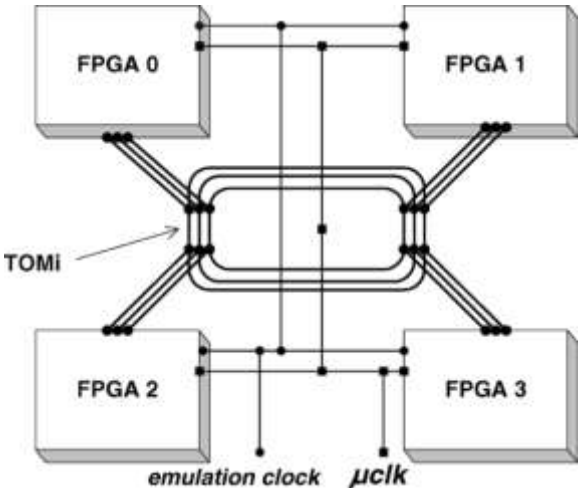
The proposed multi-FPGA structure (MS) is compared to a group of alternative concepts. They can be classified by their routing resources, switch routing delays and wave-based pin multiplexing capabilities. The MS has no routing limitations as well as the MP4 a common maximum number of traces between FPGAs in standard switch based concepts [13] is 700.Athird group of routing resources is tri state based, This determined by the pin multiplexing delay and if wave pipelining is possible—the wave-based pin multiplexing delay.

ATOMI ALGORITHM

The interconnection among FPGAs consists of wires for “emulation clock,” “_clk,” and TOMi, respectively. _clk, which is of higher frequency than emulation clock, controls micro-operations

for the signal transfer between consecutive edges of emulation clock. TOMi is composed of wires that transfer logic signals from one FPGA to another according to _clk. Each bit line of TOMi shared by all FPGAs transfers a logic signal driven by one of FPGA sin one clk cycle. It is a bidirectional signal where the signal is driven by a single source and transferred to multiple destination FPGAs. Therefore, multi terminal inter-FPGA nets can be easily routed.

Atomi structure



SIMULATION RESULT

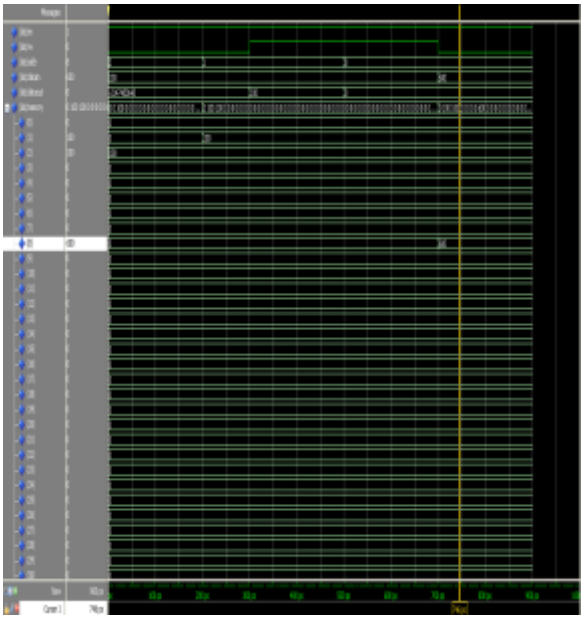


Figure 7 Transmitter and Receiver

In this waveform for corresponding input output is obtained the clock signal is unchangeable but the testing inputs varies for each routing by this routing path is calculated using all to all routing for each input delay is provided in range of nano seconds. At first input pin is forced values are changed, clock is set to delay seconds

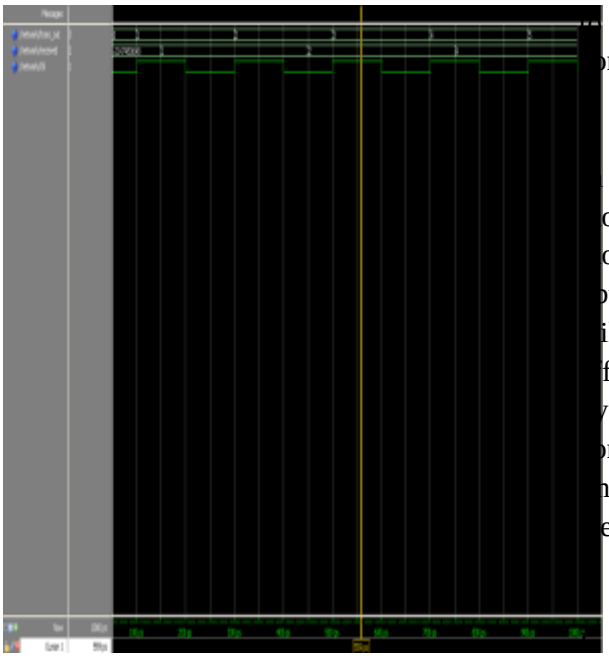


FIGURE 8 NETWORK

The above waveform indicates for corresponding input output is obtained the clock signal is unchangeable but the testing inputs varies for each routing by this routing path is calculated using Many to one routing for each input delay is provided in range of nano seconds.

CONCLUSION

The proposed multi-FPGA structure (MS) is compared to a group of alternative concepts. They can be classified by their routing resources, switch routing delays and wave-based pin multiplexing capabilities. The MS has no routing limitations as well as the MP4. A common maximum number of traces between FPGAs in standard switch based concepts .A third group of routing resources is tri state based The is determined by the pin multiplexing delay and if wave pipelining is possible the wave-based pin multiplexing delay. The proposed structure allows self-timed wave-based pin multiplexing. Wave based pin multiplexing is not possible at the MP4 and at the ATOMi, but a certain extent in the standard routing oncept.

FUTURE SCOPE

the first phase partition coding is created odules are generated and executed using odelsim also corresponding waveform is btained. In the second phase, other modules ill be simulated and integrated. Apart from this fficient routing path is determined. This is done y calculating memory size, power nsumption. Finally all the modules will be mplemented in Cyclone-IV FPGA evelopment kit.

ACKNOWLEDGEMENT

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